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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,256	06/29/2004	Zachary E. Berndlmaier	FIS920040075US1	4255

29154 7590 12/21/2005

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,256	BERNDLMAIER ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *15-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-14, in the reply filed on December 7, 2005 is acknowledged.

Claim Rejections - 35 USC § 102/35 USC § 103

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Assaderaghi et al. '907 or, in the alternative, under 35 U.S.C. 103(a) as being obvious over Assaderaghi et al. '907 in view of Adkisson et al. '913.

Assaderaghi et al. discloses a silicon-on-insulator (SOI) integrated circuit comprising a bulk region having a plurality of decoupling capacitors, wherein the decoupling capacitors include capacitive fingers extending vertically into the bulk region in a direction perpendicular to the horizontal upper surface of the bulk region (fig. 7, 18); the decoupling capacitors comprising trenches lined with an insulator

(19) and filled with a conductor (20); a common plate in the bulk region below the capacitive fingers (16); an upper interconnect plate connected to the conductor within the capacitive fingers (fig. 8, 25); a bulk contact adapted to bias the bulk region (18a); and the decoupling capacitors comprising a storage element of a DRAM element (col. 4, lines 14-21). Assaderaghi et al. does not explicitly disclose an active region comprising active switching devices on the SOI integrated structure, but the reference does teach the capacitor device to be integrated into logic technologies and other high performance circuits (col. 2, lines 22-20). According to well established logic circuit principles, it is inherent that the upper interconnect plate would extend from the decoupling capacitor into an active region in order for the DRAM element to perform its intended function.

Alternatively, assuming *arguendo* that even if connecting the upper plate of the decoupling capacitor to an active switching device was not necessary for the DRAM element to perform its intended function, it would nonetheless have been obvious to connect the upper plate of the decoupling capacitor to an active switching device. Adkisson et al. teaches a silicon-on-insulator DRAM structure comprising an active region comprising active switching devices and a bulk region comprising decoupling capacitors (fig. 8), wherein the decoupling capacitors include capacitive fingers extending into the bulk region and the upper plate of the capacitor is connected to the active devices (¶ 12, 37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the upper plate of the decoupling capacitor as described by Assaderaghi et al. to the active switches as taught by

Adkisson et al. in order to read and write information to the capacitor, which would have allowed the device to perform its intended function.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chittipeddi et al. '381 discloses a trench capacitor in a silicon-on-insulator substrate.

Davari et al. '122 discloses a buried capacitor in a silicon-on-insulator structure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
12/14/05

BRADLEY K. SMITH
PRIMARY EXAMINER